

U.S. Provisional Application Serial Number 60/180,907 filed February 8, 2000.

### REMARKS

Claims 1-51 are pending in the captioned Application in which claims 1-51 are subject to a restriction requirement.

#### RESTRICTION REQUIREMENT:

The Examiner has required restriction/election of claims as between Group I including claims 1-15 drawn to an electronic package, Group II including claims 16-36 drawn to an interposer, and Group III including claims 37-51 drawn to a method for making the interposer.

Applicant hereby elects claims 16-36 of Group II with traverse.

#### Between Group I and Group II:

Claims 1-15 of Group I are directed to an electronic package comprising at least one electronic device and a solderable flexible adhesive interposer having certain recited features.

Claims 16-36 of Group II are directed to a solderable flexible adhesive interposer having the same certain recited features as the solderable flexible adhesive interposer recited in claims 1-15. It is submitted that at least claim 1 of Group I and at least claim 16 of Group II require the same particulars for patentability and so restriction as between Groups I and II is improper and should be withdrawn.

The Examiner alleges that "the combination as claimed does not require the particulars of the subcombination as claimed because the package does not require a conductor residing between at least two of said adjacent layers." Applicant respectfully traverses. Firstly, the recitation "at least one layer of a flexible dielectric adhesive" of claim 1, for example, of Group I covers one, two, three or more layers and so is not distinct from the "plurality of layers of flexible dielectric adhesive" recited, for example, in claim 23 of Group II. Thus, a proper search must include prior art having plural layers.

Moreover, claim 5 of Group I recites "patterned metal conductors on one surface of

said layer of flexible dielectric adhesive fanning out from at least ones of said conductive vias..." and so a proper search must consider prior art having conductors on the surface of a layer, whether that layer be one or be one of plural layers.

Examiner alleges that the "subcombination has separate utility such as the interposer can be used with other semiconductor die. Applicant respectfully traverses. Applicant's claim 1 recites "an electronic device" as do various other Group I claims depending therefrom. An "electronic device" is also recited, for example, in claims 16, 17, 22, 23, 2429, 30 and 36 of Group II. It is noted that "electronic device" is a broad term that includes many different types of electronic parts including, *inter alia* a semiconductor die or chip. Thus the scope of the recited electronic device includes semiconductor die of any type, and so the utility of the interposer of Group II includes a package as recited in Group I. Examiner has provided no example of any suggested utility not encompassed by the claims of both Group I and Group II, and so the restriction requirement should be withdrawn.

Moreover, examination of the claims of Groups I and II in the present Application is consistent with both the extent of a proper search and with other patents. A proper search must encompass prior art relating to interposers of one and plural layers and utilized with a wide variety of electronic devices and substrates. In fact, claims 22 and 29 of Group II recite an interposer in combination an electronic device which includes elements similar to those of at least claim 1 of Group I. Thus, the elements of the electronic package of Group I and of the interposer of Group II are similar and so the searching required for examination of all of the claims of Groups I and II is not substantially greater that is examining only the claims of either Group I or Group II.

Further, examination of the claims of Groups I and II is consistent with PTO practice in many other applications relating to similar technology. For example, U.S. Patents 6,288,905 and 6,376,769, which issued from the priority applications in the present application, both include descriptions and claims directed to both combination and subcombination as the case with respect to the claims of Groups I and II of the present application. In fact, U.S. Patent 6,376,769 includes claims directed to an interposer, and to an electronic package including an interposer.

Accordingly, the restriction should be withdrawn at least as to the claims 1-36 of Groups I and II.

Between Groups I & II and Group III:

Claims 37-51 of Group III are directed to a method for making a solderable flexible adhesive interposer having certain recited features, which features are similar to those of the claims of Groups I and II.

Applicant notes that, for example, claim 1 directed to an electronic package comprises elements that are substantially like the elements recited, for example, in method claim 37. As a specific example:

CLAIM 1 — Electronic Package	CLAIM 37 — Method for Making...
at least one layer of flexible dielectric adhesive having a modulus of elasticity less than about 35,000 kg/cm <sup>2</sup> (about 500,000 psi)	providing at least one layer of a flexible dielectric adhesive having a modulus of elasticity less than about 35,000 kg/cm <sup>2</sup> (about 500,000 psi) on one surface of the sheet of metal foil
a plurality of conductive vias through said layer of flexible dielectric adhesive, said plurality of conductive vias being of a flexible electrically conductive adhesive having a modulus of elasticity less than about 35,000 kg/cm <sup>2</sup> (about 500,000 psi) and being in a pattern corresponding to a pattern of contacts of one of said electronic device and a substrate	providing a plurality of bumps of flexible electrically conductive adhesive having a modulus of elasticity less than about 35,000 kg/cm <sup>2</sup> (about 500,000 psi) on the metal foil at locations of the via openings of said layer of flexible dielectric adhesive, thereby forming conductive vias therein
a solderable electrically conductive metal formed on at least one exposed surface of said conductive vias and in electrical contact therewith	plating a solderable metal on an exposed end of the conductive vias to provide solderable contacts

Thus, the elements of the electronic package and of the method are similar and so the searching required for examination of all of the claims pending is not substantially greater than is examining only the claims of Group I and II, for example.

In addition, it is submitted that extent of the search required for examining either the Group I, Group II or Group III claims is not substantially different from that required for examining all the claims because the references that disclose the article also in many instances also describe the method for making the article. For example, U.S. Patents 6,288,905 and 6,376,769, which issued from the priority applications in the present application, both include claims directed to both an article and to the method for making the article as the case with respect to the claims of Groups I, II and III of the present application. In fact, U.S. Patent 6,376,769 includes claims directed to an interposer, to a package including an interposer, and to a method for making the package. Other references cited in U.S. Patent 6,376,769 are similar. For example, the Yamaji and the Okoshi et al references describe both the prior art article and the method for making the prior art article.

Further, examination of the claims of Group III along with the claims of Groups I and II is consistent with PTO practice in many other applications relating to similar technology, for example, the patents referred to in the immediately preceding paragraph.

Accordingly, it is requested that the restriction be withdrawn and all of Applicant's claims be examined in the present Application.

AMENDMENT TO THE SPECIFICATION:

The specification is amended at page 1 to also include a claim to the priority of U.S. Provisional Application Serial Number 60/180,544 filed February 7, 2000. Applicant hereby claims the priority thereof in the present Application, and requests that the record reflect such claim. Changes to the paragraph amended are shown in the Appendix hereto.

CONCLUSION:

No fee is due in this timely-filled response. Should any fee be due in consequence of this response, please charge such fee and deposit any refund to Deposit Account 04-1406.

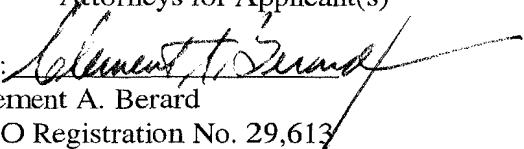
Applicant respectfully requests that the restriction be withdrawn, and that the Application including claims 1-51 be examined, allowed and passed to issuance.

AI-TECH-16A

PATENT APPLICATION  
Serial No. **09/578,583**

The Examiner is requested to telephone the undersigned attorney if there is any question or if prosecution of this Application could be furthered by telephone.

Respectfully submitted,  
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## APPENDIX

### SPECIFICATION PARAGRAPH(S) SHOWING AMENDED WORDING:

Paragraph beginning at page 1, line 4:

This Application is a continuation-in-part of U.S. Patent Application Serial Number 09/412,052 filed October 4, 1999 and of U.S. Patent application Serial Number 09/524,148 filed March 14, 2000, and claims the benefit of U.S. Provisional Application Serial Number 60/136,917 filed June 1, 1999, of U.S. Provisional Application Serial Number 60/141,344 filed June 28, 1999, of U.S. Provisional Application Serial Number 60/150,437 filed August 24, 1999, of U.S. Provisional Application Serial Number 60/150,869 filed August 26, [1999.and] 1999, of U.S. Provisional Application Serial Number 60/180,544 filed February 7, 2000, and of U.S. Provisional Application Serial Number 60/180,907 filed February 8, 2000.